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Claims

[c1] A durable chip pad comprising:
a terminal metal layer disposed on a passivating layer;
a diffusion barrier layer on said terminal metallurgy layer;
a conducting layer on said diffusion barrier
a hard test barrier layer on said conducting barrier layer; and
a plate passivating layer on said hard test barrier layer.

[c2] A durable chip pad as in claim 1, wherein said diffusion barrier layer includes an adhesion layer on barrier metallurgy.

[c3] A durable chip pad as in claim 2, wherein said barrier metallurgy is selected from a group of metals and metal alloys comprising titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), chromium (Cr) and tantalum/tantalum nitride (Ta/TaN).

[c4] A durable chip pad as in claim 3, wherein said adhesion layer is selected from a group of metals and metal alloys comprising chrome-copper (CrCu), nickel vanadium (NiV) and titanium (Ti).

[c5] A durable chip pad as in claim 1, wherein said hard test barrier layer comprises a nickel (Ni) layer.

[c6] A durable chip pad as in claim 5, wherein said hard test barrier layer further comprises a copper layer, said nickel layer being plated to said copper layer.

[c7] A durable chip pad as in claim 1, wherein said plate passivating layer is selected from a group of metals comprising copper (Cu), ruthenium (Ru), rhodium (Rh) and gold (Au).

[c8] An integrated circuit (IC) chip with circuits formed thereon, a plurality of chip interconnect pads formed on a surface of said IC chip, one or more of said plurality of chip interconnect pads being a durable chip pad comprising:
a terminal metal layer disposed on a chip passivating layer and connecting to underlying chip wiring through a via through said chip passivating layer;
an adhesion/barrier layer on said terminal metallurgy layer;
a seed layer on said adhesion/barrier layer;
a hard test barrier layer on said diffusion barrier layer; and
a plate passivating layer on said hard test barrier layer.

[c9] An IC as in claim 8, wherein said adhesion/diffusion barrier layer includes an adhesion layer on barrier metallurgy and said barrier metallurgy is selected from a group of metals and metal alloys comprising titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), chromium (Cr) and tantalum/tantalum nitride (Ta/TaN).

[c10] An IC as in claim 9, wherein said adhesion layer is selected from a group of metals and metal alloys comprising chrome-copper (CrCu), nickel vanadium (NiV) and titanium (Ti).

[c11] An IC as in claim 10, wherein said seed layer comprises a copper layer.

[c12] An IC as in claim 11, wherein said hard test barrier layer comprises a nickel (Ni) layer.

[c13] An IC as in claim 12, wherein said plate passivating layer is selected from a group of metals comprising copper (Cu), ruthenium (Ru), rhodium (Rh) and gold (Au).

[c14] An IC as in claim 13, wherein said IC is one of a plurality of identical ICs on a wafer, each of said plurality of identical ICs located in a die on said wafer.

[c15] A method of forming integrated circuit (IC) chips on a semiconductor wafer, said method comprising the steps

of:

a) forming ICs in die locations on a semiconductor wafer, said die locations including a plurality of terminal metallurgy pads;

b) forming seed layers on said semiconductor wafer;

c) forming seed pads from said seed layers;

d) forming a hard test barrier on said seed pads;

e) passivating said hard test barrier on said pads; and

f) removing remaining material between passivated said pads, durable pads remaining on said wafer at said terminal metallurgy pads.

[c16] A method of forming IC chips as in claim 15, wherein the step (b) of forming the seed layers comprises:

i) forming an adhesion/barrier layer on said semiconductor wafer; and

ii) forming a seed layer on said adhesion/barrier layer.

[c17] A method of forming IC chips as in claim 16, wherein forming said seed layer comprises forming a layer terminating in copper.

[c18] A method of forming IC chips as in claim 16, wherein the step (c) of forming seed pads comprises:

i) forming a block out mask on said seed layer; and

ii) selectively removing exposed portions of said seed layer.

[c19] A method of forming IC chips as in claim 17, wherein seed layer is a copper layer and the step (d) of forming a hard test barrier comprises plating a nickel layer on said copper seed pad.

[c20] A method of forming IC chips as in claim 15, further comprising the step of:
g)testing each formed one of said IC chips by application of test probes directly to said durable pads.